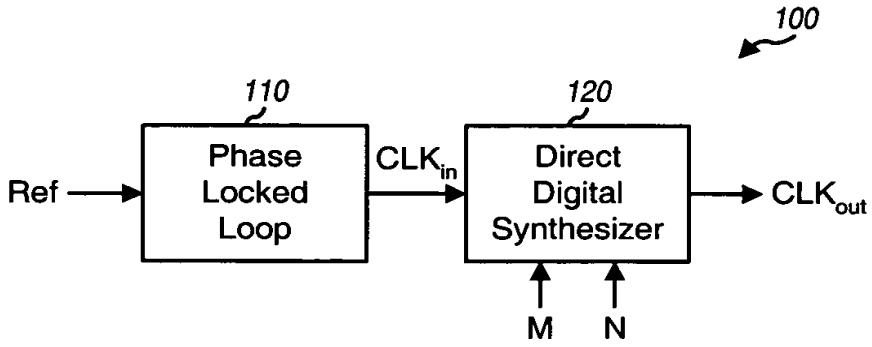
100
110
120
Ref
Phase Locked Loop
CLK$_{in}$
Direct Digital Synthesizer
CLK$_{out}$
M
N

FIG. 1

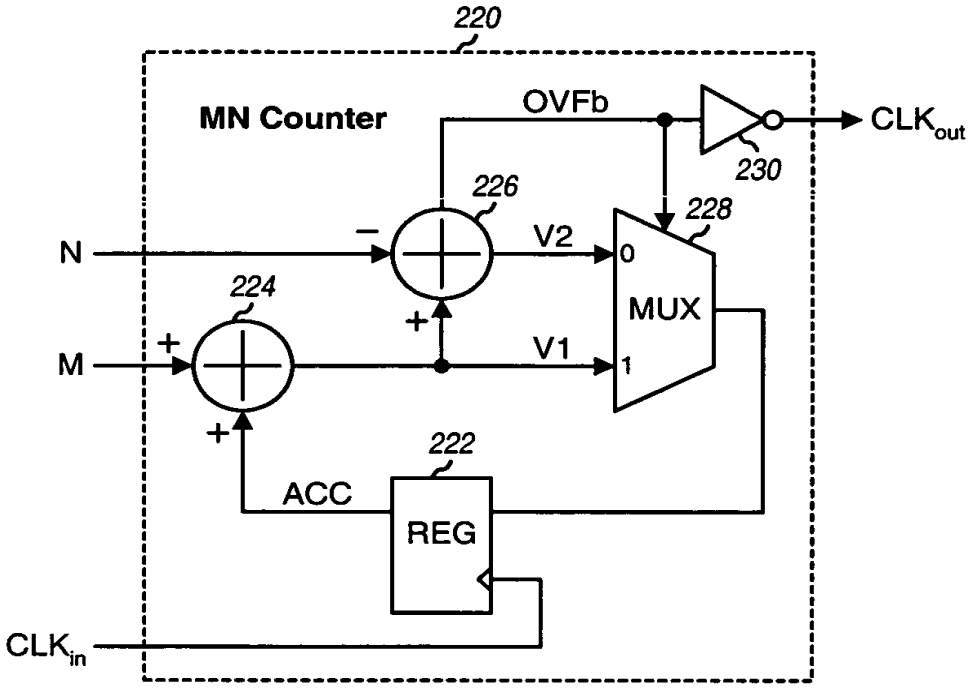
220
MN Counter
OVFb
CLK$_{out}$
230
226
228
N
V2
0
MUX
224
M
V1
1
222
ACC
REG
CLK$_{in}$

FIG. 2

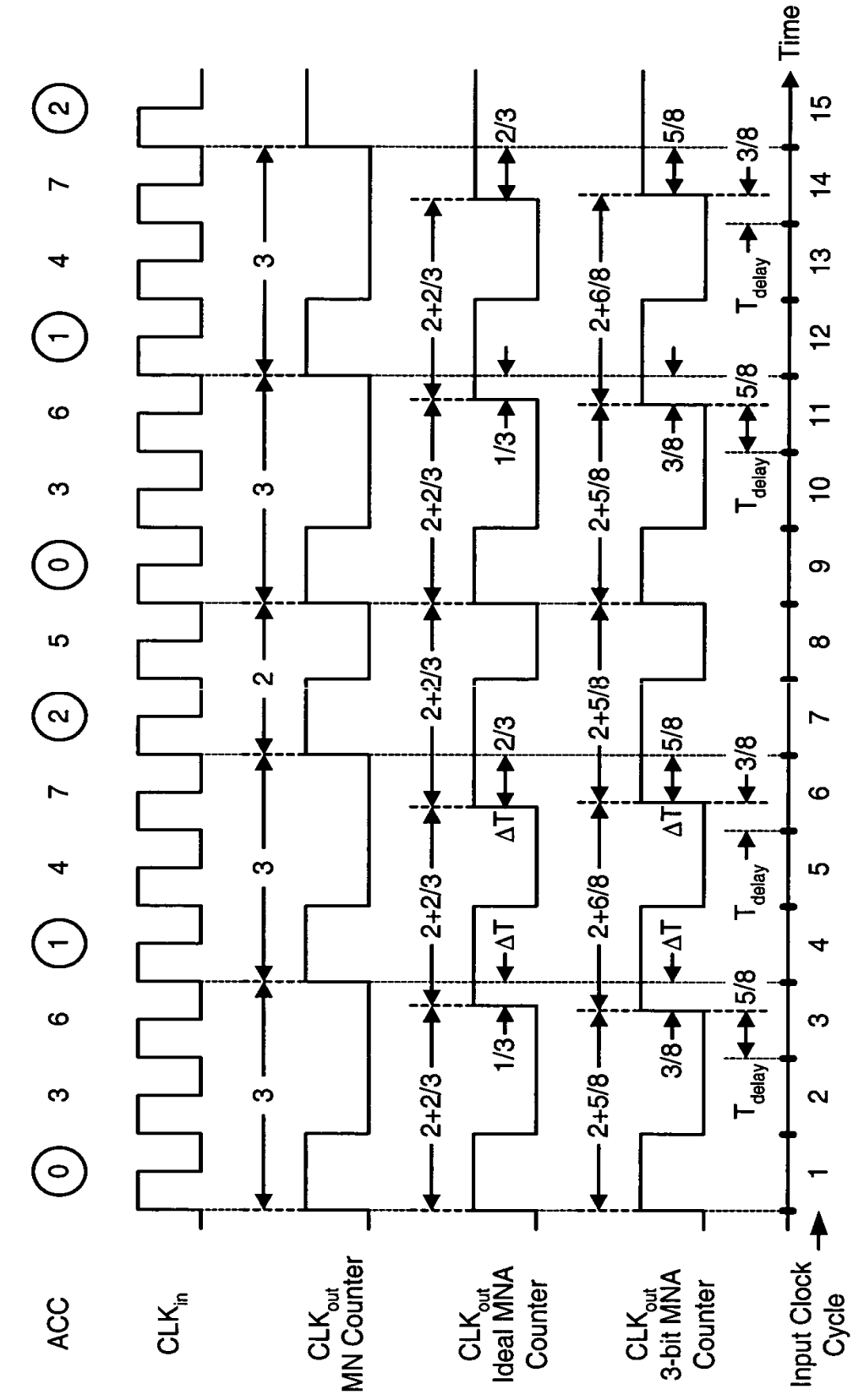
ACC
0
3
6
1
4
7
2
5
0
3
6
1
4
7
2
CLK$_{in}$
CLK$_{out}$ MN Counter
CLK$_{out}$ Ideal MNA Counter
CLK$_{out}$ 3-bit MNA Counter
Input Clock Cycle
Time
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
3
2
2+2/3
1/3
ΔT
2/3
2+5/8
3/8
5/8
2+6/8
T$_{delay}$

FIG. 3

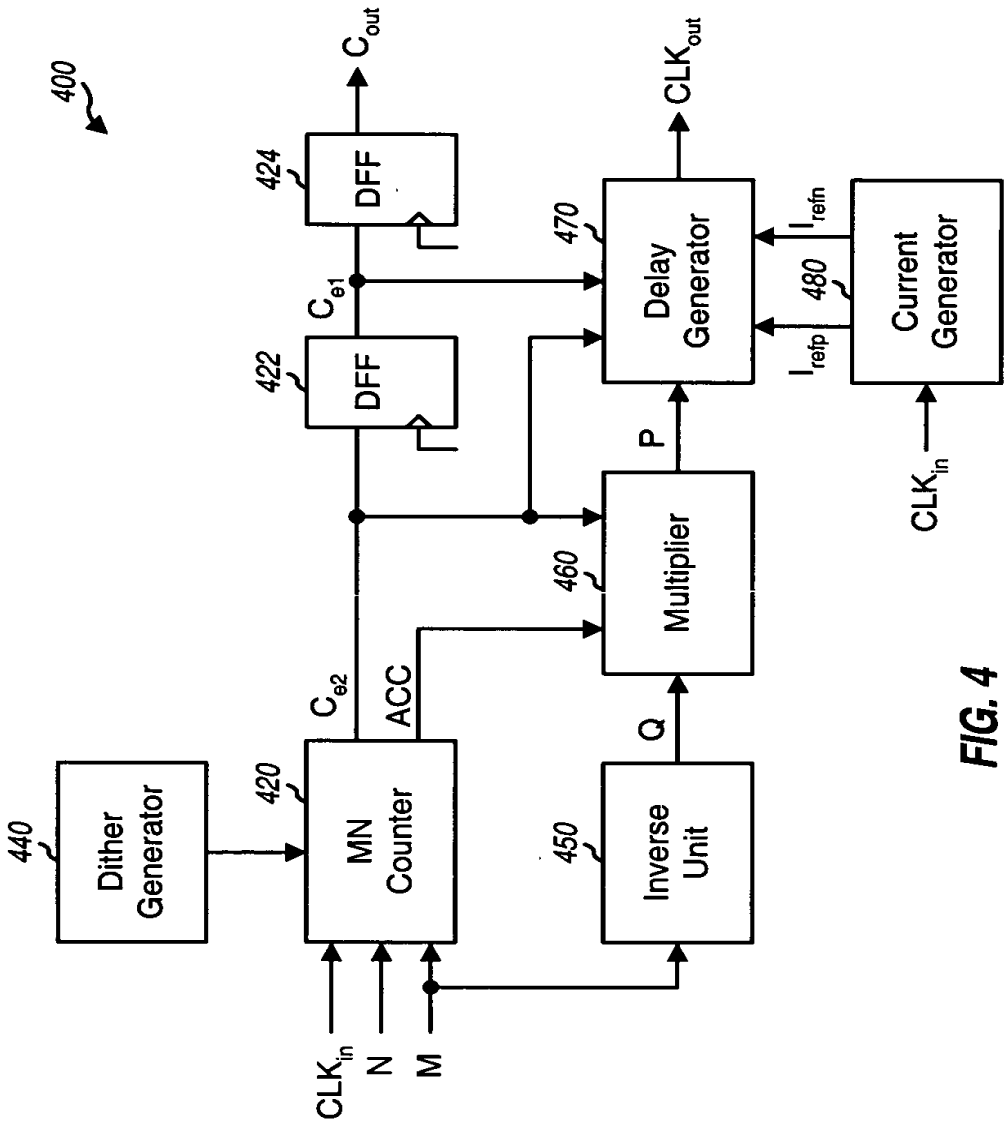
400
440
Dither Generator
420
MN Counter
422
DFF
424
DFF
450
Inverse Unit
460
Multiplier
470
Delay Generator
480
Current Generator
CLK_in
N
M
C_e2
ACC
C_e1
C_out
Q
P
CLK_out
I_refn
I_refp
CLK_in

FIG. 4

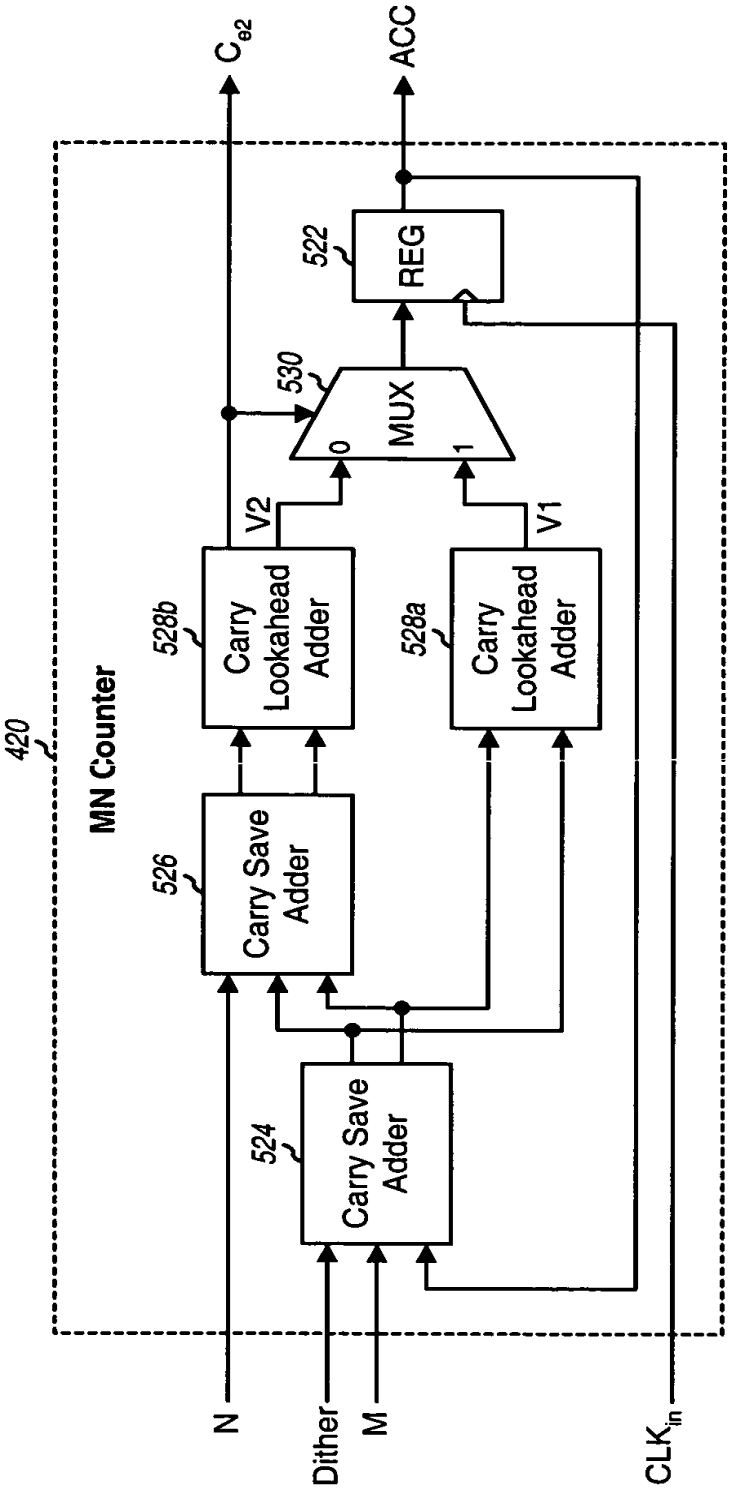
C_{e2}
ACC
522
REG
530
MUX
0
1
V2
V1
528b
Carry Lookahead Adder
528a
Carry Lookahead Adder
526
Carry Save Adder
524
Carry Save Adder
420
MN Counter
N
Dither
M
CLK_{in}

FIG. 5

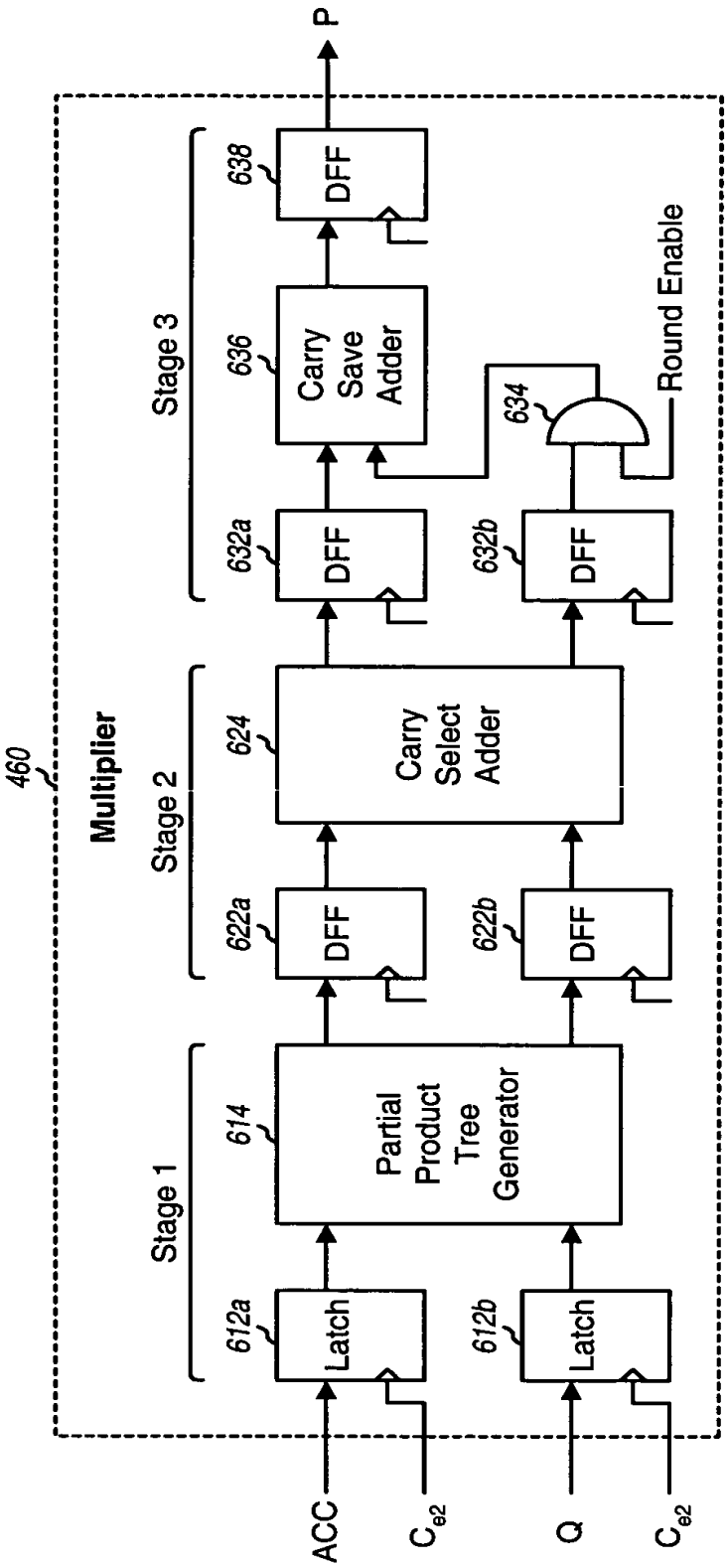
460
Multiplier
Stage 1
Stage 2
Stage 3
612a
Latch
612b
Latch
614
Partial Product Tree Generator
622a
DFF
622b
DFF
624
Carry Select Adder
632a
DFF
632b
DFF
634
636
Carry Save Adder
638
DFF
Round Enable
P
ACC
C_{e2}
Q
C_{e2}

FIG. 6

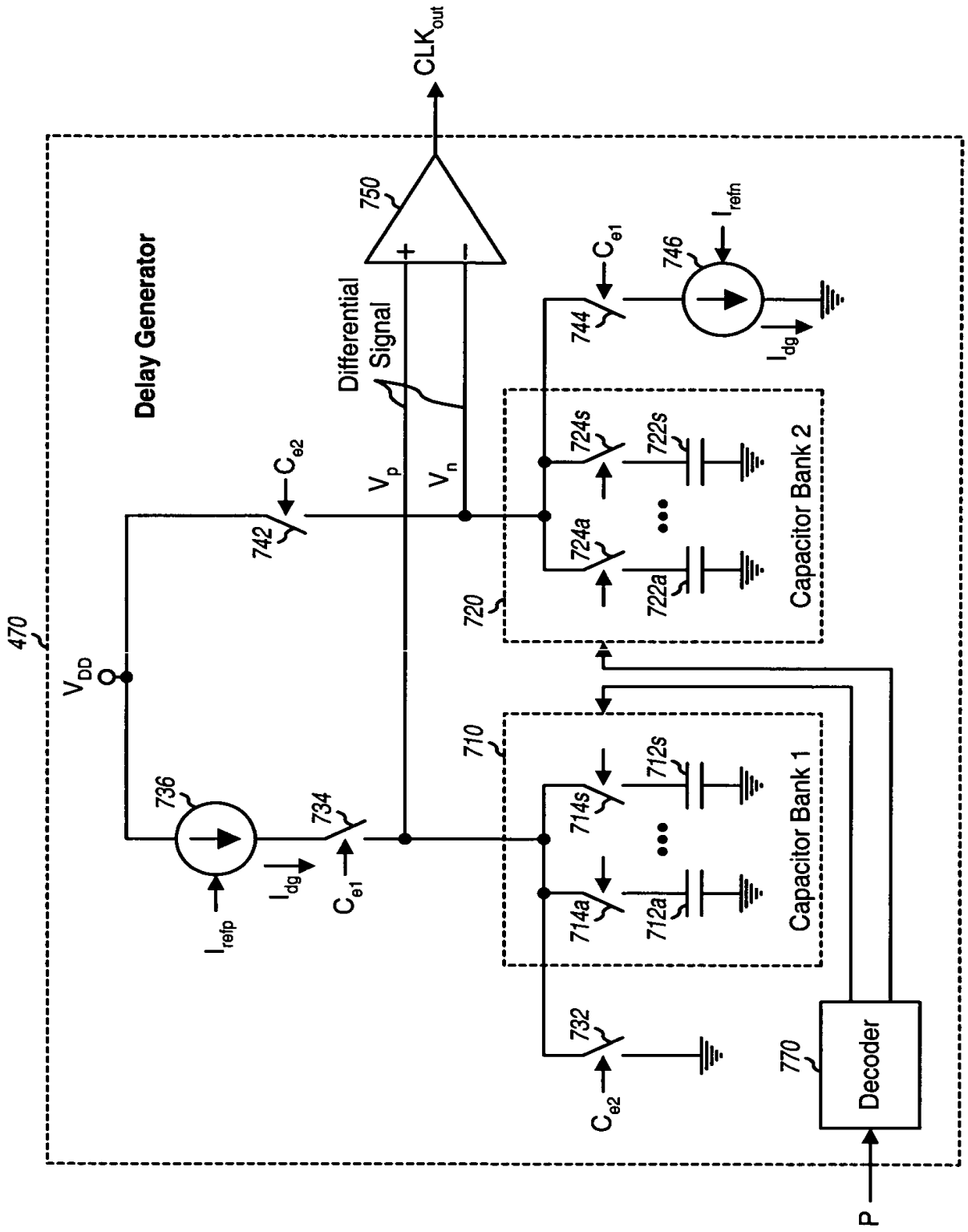
Delay Generator
470
V_{DD}
736
I_{refp}
I_{dg}
734
C_{e1}
742
C_{e2}
V_p
V_n
Differential Signal
750
CLK_{out}
710
Capacitor Bank 1
712s
712a
714s
714a
732
C_{e2}
720
Capacitor Bank 2
722s
722a
724s
724a
744
C_{e1}
746
I_{refn}
I_{dg}
770
Decoder
P

FIG. 7

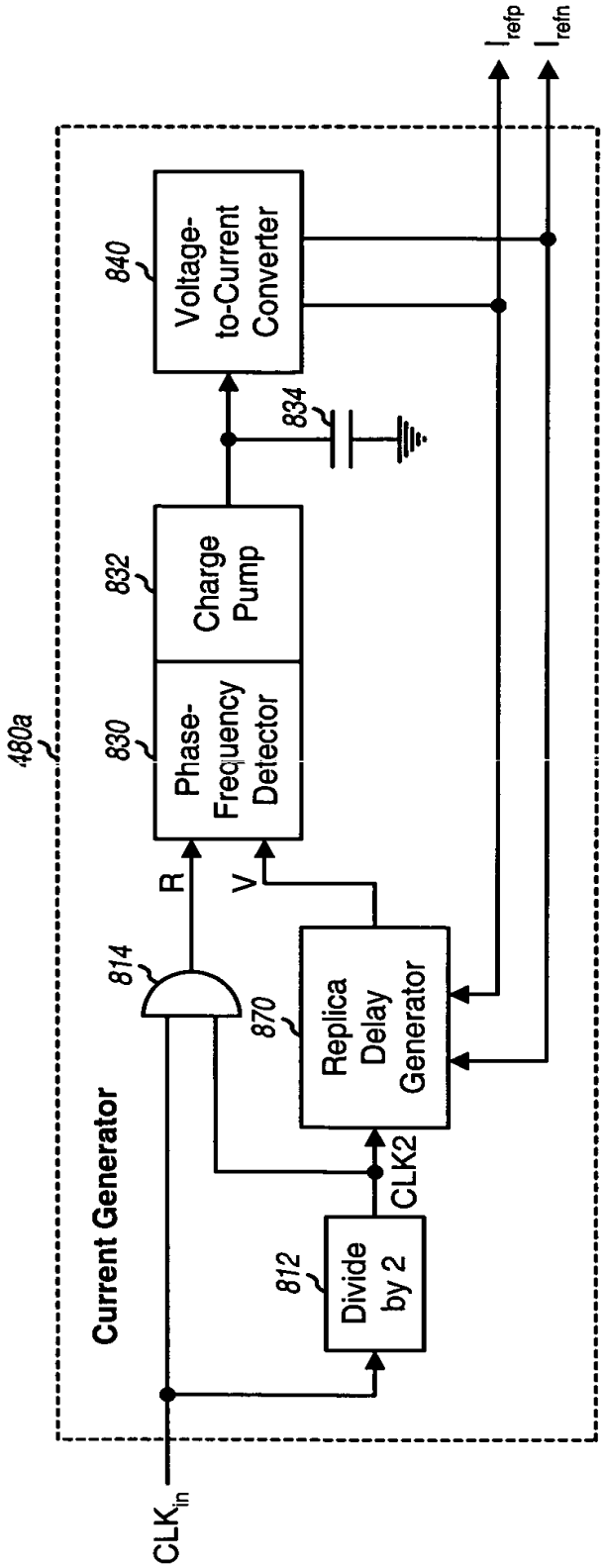
480a
Current Generator
CLK$_{in}$
812
Divide by 2
CLK2
814
870
Replica Delay Generator
R
V
830
Phase-Frequency Detector
832
Charge Pump
834
840
Voltage-to-Current Converter
I$_{refp}$
I$_{refn}$

FIG. 8A

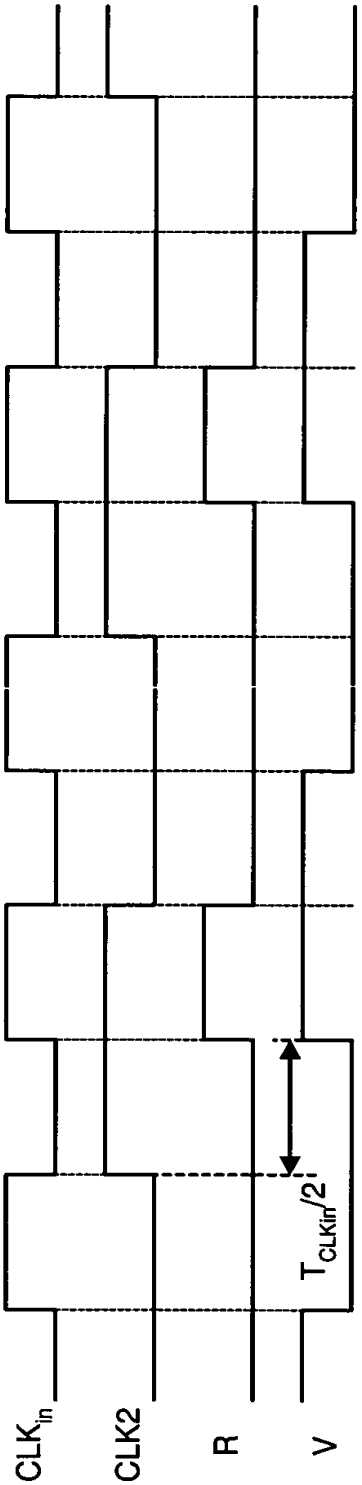
CLK$_{in}$
CLK2
R
V
T$_{CLKin}$/2

FIG. 8B

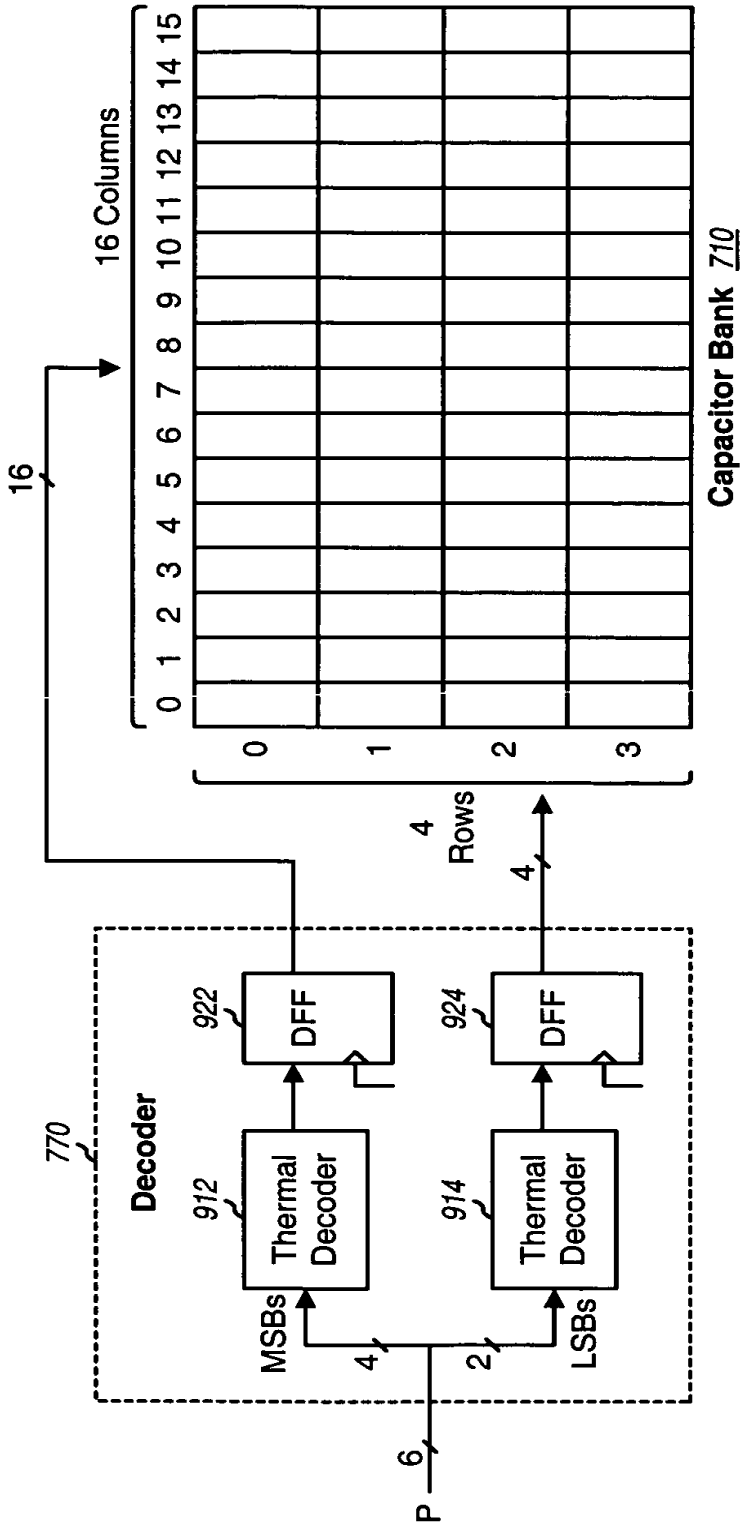
16 Columns
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
16
0
1
2
3
4 Rows
Capacitor Bank 710
4
922
DFF
924
DFF
770
Decoder
912
Thermal Decoder
914
Thermal Decoder
MSBs
LSBs
4
2
6
P

FIG. 9

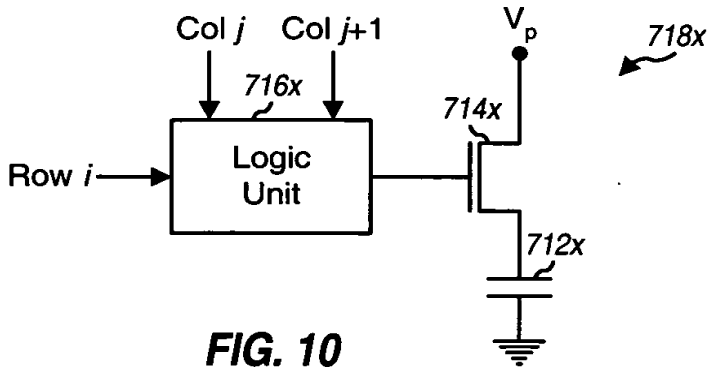
Col j
Col j+1
716x
Row i
Logic Unit
V_p
718x
714x
712x

FIG. 10

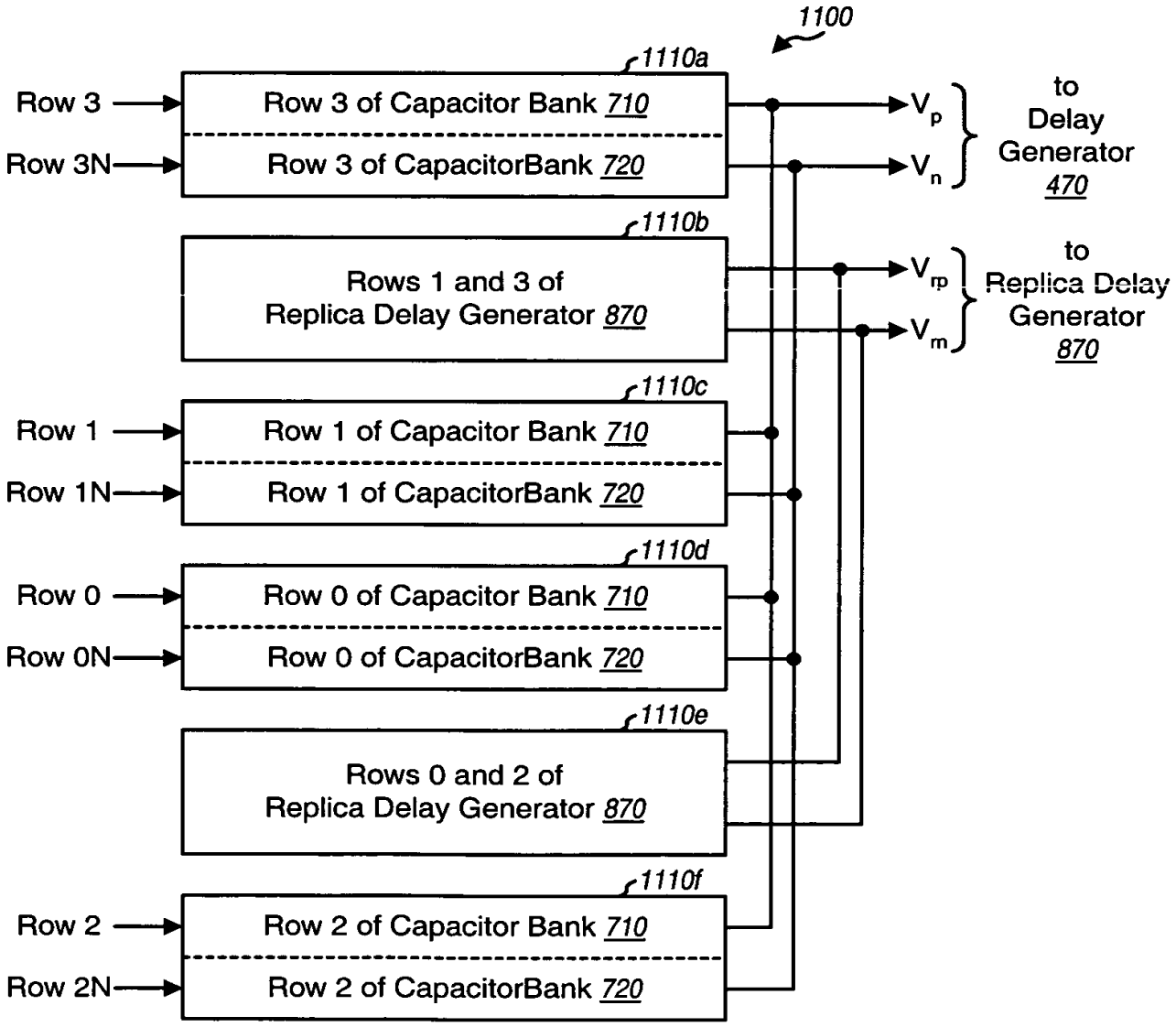
1100
1110a
Row 3
Row 3N
Row 3 of Capacitor Bank 710
Row 3 of CapacitorBank 720
V_p
V_n
to Delay Generator 470
1110b
Rows 1 and 3 of Replica Delay Generator 870
V_{rp}
V_{rn}
to Replica Delay Generator 870
1110c
Row 1
Row 1N
Row 1 of Capacitor Bank 710
Row 1 of CapacitorBank 720
1110d
Row 0
Row 0N
Row 0 of Capacitor Bank 710
Row 0 of CapacitorBank 720
1110e
Rows 0 and 2 of Replica Delay Generator 870
1110f
Row 2
Row 2N
Row 2 of Capacitor Bank 710
Row 2 of CapacitorBank 720

FIG. 11

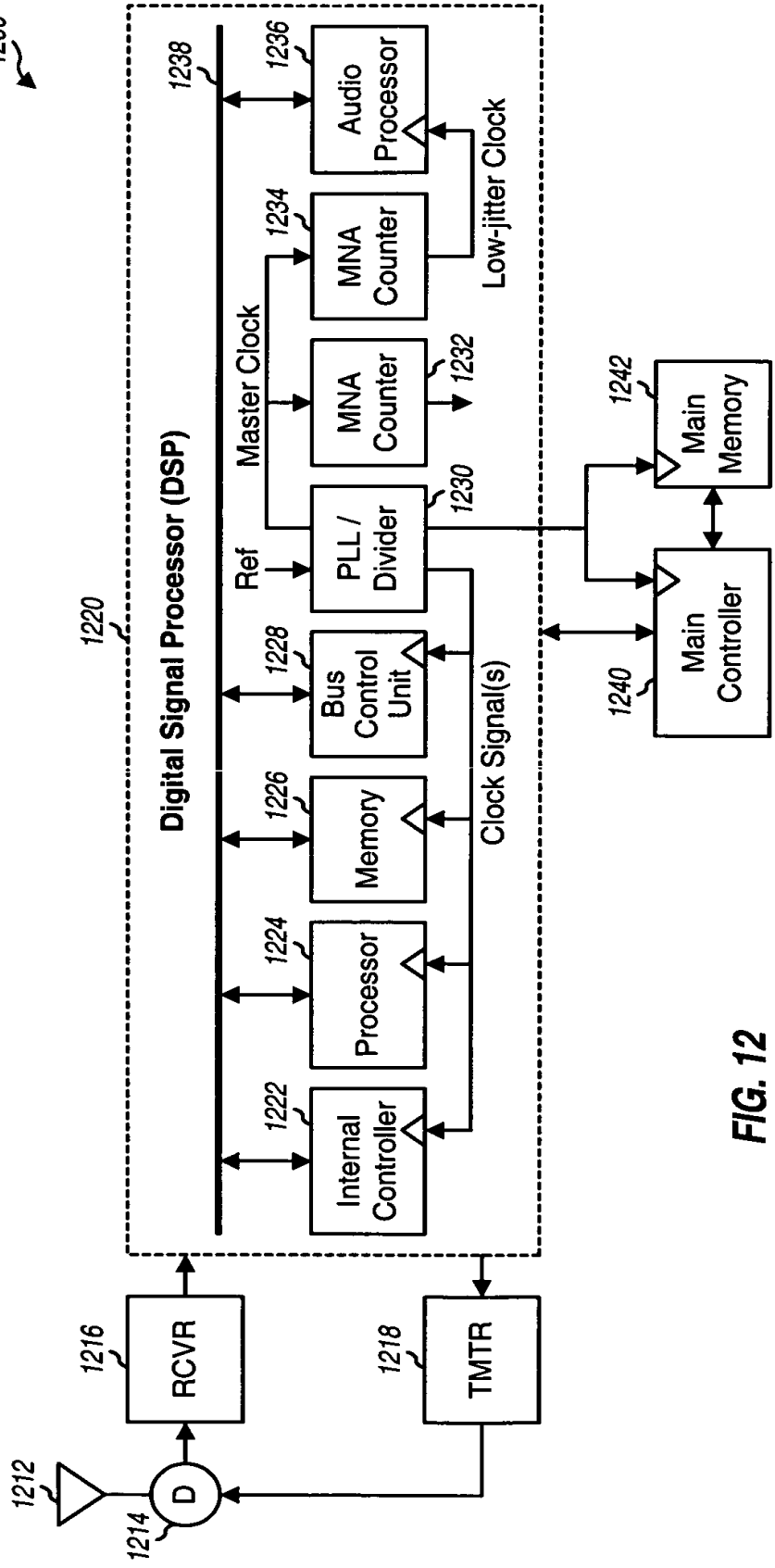
1200
1220
Digital Signal Processor (DSP)
1238
1236
Audio Processor
1234
MNA Counter
Low-jitter Clock
Master Clock
1232
MNA Counter
1230
Ref
PLL / Divider
1228
Bus Control Unit
1226
Memory
1224
Processor
1222
Internal Controller
Clock Signal(s)
1242
Main Memory
1240
Main Controller
1216
RCVR
1218
TMTR
1212
1214
D

FIG. 12